adjust step-size. Referring to Fig. 1, a data signal 120 has a bit-rate that has a fixed difference with respect to a Dclk clock signal 125a or the data signal 120 has a data bit-rate that varies continuously in a range of data bit-rates with respect to the Dclk clock signal 125a. (See paragraph [0022]). Thus, Kim only discloses an apparatus for compensating for data phase drift (frequency differences) already present in an incoming data signal.

At pg. 2 of the Office Action, it is alleged that paragraph [0022] of Kim discloses the "producing test data from a first CDR" feature of claim 1. However, this portion of Kim merely discusses how the CDR circuit 100 tracks the data signal 120 having a variable bit-rate by adjusting a phase-adjust step-size. Kim provides no disclosure as to producing test data.

Further, at pg. 2 of the Office Action, it is alleged that Kim discloses, in Fig. 2, "generating data drift in the test data by changing a phase of the clock," as called for by claim 1. However, Fig. 2 of Kim is merely a graphical representation of Equ. 1, which calculates the maximum data phase drift that the CDR circuit 100 is able to tolerate. (See paragraph [0038]). Fig. 2 of Kim does not depict generating data drift in test data.

Thus, Kim fails to teach or suggest "producing test data" or "generating data drift in the test data," as called for by claim 1.

Further, Kim fails to teach or suggest "a test data generator to generate test data based on the phase variable clock," as called for by claim 10. The Office Action alleges that the data signal 120 and a data sampler 110 correspond to the test data and test data generator, respectively, of claim 10. However, the data sampler 110 merely receives the data signal 120 and cannot be said to generate test data.

Further, Kim fails to teach or suggest "the test data generator is a pseudo random number generator," as called for by claim 13. Referring to Figs. 1 and 8 of Kim, a finite state machine 800 (alleged pseudo-number generator) increments or decrements a step-size in

order to compensate for frequency differences (data drift) in the incoming data signal 120. The finite state machine does not generate test data.

Further, Kim fails to teach or suggest "the phase variable clock source is a phase rotator coupled to a phase locked loop (PLL) oscillator," as called for by claim 14. Kim discloses a phase adjust controller 114 that generates a phase adjust signal 123 in response to a step-size signal 127 that represents the amount of phase adjustment needed to shift clock signals 124a-b to produce Dclk clock signal 125b. (See paragraph [0035]). The phase adjust signal 123 is generated in order to compensate for data drift in the incoming signal 120. Thus, the phase adjust controller 114 does not correspond to the "phase rotator coupled to a phase locked loop (PLL) oscillator" of claim 14 because the phase adjust controller 114 is not a phase variable clock source on which test data generated by a test data generator is based.

Further, Kim fails to teach or suggest, for at least the same reasons discussed above with respect to claim 10, "a system or a network implementing the CDR of claim 10," as called for by claim 15. Kim fails to teach or suggest the features of claim 10, and thus fails to teach or suggest a system or a network implementing the CDR of claim 10.

Further, Kim fails to teach or suggest "means for generating test data" or "means for producing a range of data drift conditions in the test data by changing a phase of the clock," as called for by claim 16.

As discussed above, Kim fails to teach or suggest generating test data or producing a range of data drift conditions in the test data. Kim only discloses an apparatus that compensates for data drift already present in an incoming data signal. Further, the phase adjust controller 114 does not correspond to the "means for producing a range of data drift conditions in the test data by changing a phase of the clock" of claim 16 for at least the same reasons discussed above with respect to claim 13. The phase adjust controller 114 adjusts a

phase of a clock signal in order to compensate for data drift in an incoming signal and not to produce "a range of data drift conditions in ... test data."

Further, Kim fails to teach or suggest "means for producing a range of data drift conditions include means for reducing a rate of data drift," as called for by claim 17. As discussed above with respect to claim 16, Kim fails to teach or suggest "means for producing a range of data drift conditions in the test data," and thus fails to teach or suggest means for reducing a rate of data drift in the test data.

Further, Kim fails to teach or suggest, for at least the same reasons discussed above with respect to claims 1 and 16, "a first CDR having a test data generator and a finite state machine to adjust data drift in the test data by setting a phase of a clock based," as called for by claim 18. The state machine 800 adjusts the step-size to compensate for data drift already present in the incoming data signal 120. Kim does not teach or suggest test data generation, and thus the state machine 800 does not adjust data drift in test data.

Accordingly, withdrawal of the rejection is respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Srikant Viswanadham
Registration No. 60,111

JAO:SQV/mrh

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OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

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